



Image B

Docket No.: 57454-329

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of : Customer Number: 20277  
Masahiro SHIMIZU, et al. : Confirmation Number: 3990  
Serial No.: 10/053,543 : Group Art Unit: 2814  
Filed: January 24, 2002 : Allowed: October 27, 2003  
: Examiner: G. Peralta

For: INTEGRATED CIRCUIT HAVING A MEMORY CELL TRANSISTOR WITH A GATE OXIDE LAYER WHICH IS THICKER THAN THE GATE OXIDE LAYER OF A PERIPHERAL CIRCUIT TRANSISTOR (As Amended)

**REQUEST FOR COMPLETE ACKNOWLEDGEMENT OF THE CITED ART**

Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

We are in receipt of the Notice of Allowance dated October 27, 2003.

In reviewing the file, it is noted that we have not received a **complete** acknowledgement of the Information Disclosure Statement and cited art filed January 24, 2002.

Applicants note the Examiner acknowledged receipt of the Information Disclosure Statement (IDS) but only included a partially initialed copy of Form PTO-1449 indicating consideration of the references with the exception of the Japanese references. Applicants would request the Examiner to clarify the record by providing an appropriately initialed copy of Form PTO-1449 indicating consideration of each of the cited references, including the Japanese references. In this respect, Applicants would

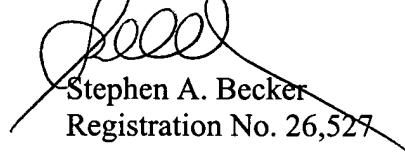
note that in the parent Application, the same Japanese references were considered by the Examiner.

For the Examiner's convenience, a copy of the incompletely acknowledged 1449 is enclosed and those references not initialed are highlighted.

It is respectfully requested that the record be clarified to confirm that the cited art has been considered and made of record.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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**Date: December 1, 2003**